Amendments to the Drawings

The attached new sheets of drawings includes Figs. 9-11 which are submitted in response to the Examiner's objection to the drawings

Attachment: New Sheets

REMARKS

At the time of the Office Action dated September 14, 2005, claims 1-9 were pending in this application. In this Amendment, new claims 10 and 11 have been added. Care has been exercised to avoid new matter. Adequate descriptive support for the new claims can be found in, for example, expressions (14) and (17) in the specification.

Drawings.

The Examiner pointed out that as numerous claim limitations are focused on voltage waveform design, drawings illustrating these limitations would facilitate a better understanding of the applicant's invention.

In response, Applicant has added Figs. 9-11. No new matter has been introduced by Figs. 9-11 for the reasons set forth below.

Fig. 9 is a voltage waveform diagram of gate lines according to the first embodiment. Fig. 9 illustrates the description on page 14, lines 7-13 and 22-26 of the specification as to the voltage setting of the first gate line (GL) and the second gate line (GL#) in select and non-select states. VGL < VDLmin and VGH > VDHmax illustrated in Fig. 9 are defined by expression (6), as well as expressions (4) and (12) in the specification.

Fig. 10 is a voltage waveform diagram of the gate lines in an example where P-type TFT elements are used according to the first and second embodiments. Fig. 10 illustrates the description on page 18, lines 23-29 of the specification as to the voltage setting of the first gate line (GL) and the second gate line (GL#) in the select and non-select states when the P-type TFT elements are used.

Fig. 11 is a voltage waveform diagram of gate line GL# according to the third embodiment. Fig. 11 illustrates the description on page 19, lines 25-31 of the specification as to the voltage setting of the second gate line (GL#).

It is noted that the gate voltage setting with the first voltage, the second voltage and the third voltage recited in the last paragraph of claims 1 and 9 is exemplary illustrated in Fig. 9. The setting of the third voltage recited in claims 2 and 3 is also exemplary explained by Fig. 9 and expressions (14) and (17). The relationship in the magnitude between the first voltage (VGH) that is an on-voltage and the second voltage that is an off-voltage in an N-type TFT element recited in claim 7 is also exemplary shown in Fig. 9. Claim 4 is directed to the gate drive circuit, and does not recite any limitations related to a voltage waveform. The limitations recited in claims 5 and 6 are exemplary illustrated by Fig. 11. The relationship in the magnitude between the first voltage that is an on-voltage and the second voltage that is an off-voltage in a P-type TFT element recited in claim 8 is exemplarily shown in Fig. 10.

Accordingly, Figs. 9-11 exemplary illustrate the limitations recited in the pending claims. Applicant, therefore, respectfully solicits withdrawal of the objection to the drawings.

Claims 1, 5-7 and 9 have been rejected under 35 U.S.C. §102(b) as being anticipated by Shimada et al.

In the statement of the rejection, the Examiner asserted that Shimada et al. discloses an active matrix substrate identically corresponding to what is claimed. This rejection is respectfully traversed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed

invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See EMI Group N. Am., Inc. v. Cypress Semiconductor Corp.*, 268 F.3d 1342, 60 USPQ2d 1423 (Fed. Cir. 2001); *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

In response, Applicant submits that Shimada does not disclose a liquid crystal display apparatus including all the limitations recited in independent claims 1 and 9. Specifically, Shimada et al. does not disclose, among other things, "said gate drive circuit... setting a voltage of said first gate line in said non-select state to a second voltage that can turn-off said first field-effect transistor as well as setting a voltage of said second gate line in said non-select state to a third voltage that is intermediate between a maximum value and a minimum value of said display voltage," recited in claims 1 and 9.

Shimada et al. is directed to an active matrix substrate. The reference discloses each pixel having first and second transistors 103a, 103b to connect data line 102 to liquid crystal element 107. As shown in Fig. 2, the gates of first and second transistors 103a, 103b are applied with different voltages (see G (1,1) and G (1, 2) in Fig. 7), respectively, when in a non-select state.

The Examiner asserted that Shimada et al. describes the above limitation by citing the following portions: "[d]ifferent electric potentials can be applied to the two gate electrodes of the TFTs 103a and 103b, respectively, that the TFTs 103a and 103b are in the OFF-state" (column 3, lines 43-45); and "[e]ach of the differences between electrode potentials of respective gate electrodes of the TFTs is preferably not greater than a peak-to-peak maximum value of the video signal..." (column 5, lines 53-56).

According to the above portions, Shimada et al. appears to disclose applying different voltages to the gates of two transistors, respectively. However, Shimada et al. does not mandate use of "a voltage of said second gate line in said non-select state to a third voltage that is intermediate between a maximum value and a minimum value of said display voltage," recited in claims 1 and 9. Accordingly, the reference does not identically disclose what is claimed.

Moreover, there are further differences between the claimed invention and Shimada et al. In claim 1, a plurality of field effect transistors are serially connected between a liquid crystal element (pixel electrode) and a data line. A transistor on the data line side (first field-effect transistor) relative to the first node receives at its gate a voltage (second voltage) that can turn it off, while a transistor on the pixel electrode side (second field-effect transistor) relative to the first node receives at its gate an intermediate voltage (third voltage).

In contrast, according to Shimada et al. in Fig. 7, the transistor on the pixel electrode side does not constantly receive at its gate an intermediate voltage. Instead, the gate voltage setting in an off-state is switched between transistors (TFTs 701, 702) for every field. On the other hand, according to the claimed invention, the third voltage that is the gate voltage in a non-select state can be a constant voltage among fields, as shown by expressions (14) and (17) in the specification. New claims 10 and 11 expressly recite this arrangement.

According to the claimed invention, for the transistor on the pixel electrode side, the voltage stress to a gate insulation film is alleviated to prevent gate leakage, and thus operating reliability can be improved (page 15, lines 14-29 of the specification). In contrast, Shimada et al. cannot alleviate with higher priority voltage stress to the gate insulation film for the transistor on the pixel electrode side.

In this regard, even if gate leakage occurs due to breakdown of the insulation film at the transistor on the data line side, its effect is relatively small since an output impedance of the data line driver or that of the gate line driver is sufficiently lower than the leakage resistance. On the other hand, such gate leakage has a great effect on the transistor on the pixel electrode side, leading to loss of charges stored in the pixel electrode. Accordingly, alleviating with higher priority the voltage stress to the gate insulation film in the transistor on the pixel electrode side to prevent gate leakage provides a significant effect as in the claimed invention, as compared with the what is disclosed in Shimada et al.

Shimada et al. does not disclose a liquid crystal display apparatus including all the limitations recited in independent claims 1 and 9 within the meaning of 35 U.S.C. §102. Dependent claims 5-7 are also patentably distinguishable over Shimada et al. at least because they respectively include all the limitations recited in independent claim 1. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1, 5-7 and 9 under 35 U.S.C. §102(b), and favorable consideration thereof.

Claims 2-4 and 8 have been rejected under 35 U.S.C. §103(a).

The Examiner asserted that claims 2-4 and 8 would have been obvious over the combination of Shimada and Morozumi et al., Koden et al., Yumoto, or Kondo et al.

In response, Applicant submits that claims 2-4 and 8 are patentably distinguishable over the applied combination of the references, at least because the claims include all the limitations recited in independent claim 1. Morozumi et al., Koden et al., Yumoto, and Kondo et al. do not teach a liquid crystal display apparatus recited in claim 1, and do not cure the deficiencies of

Shimada et al. Withdrawal of the rejection of claims 2-4 and 8 under 35 U.S.C. §103 is respectfully solicited.

New claims 10 and 11.

New claims 10 and 11 are patentably distinguishable over the cited references at least because they include all the limitations recited in independent claims 1 and 9, respectively. Applicant respectfully solicits favorable consideration of new claims 10 and 11.

Conclusion.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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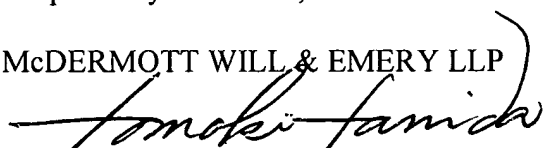

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